



INFORMATION DISCLOSURE CITATION PTO-1449	Atty. Docket No. 010704A	Serial No. 10/709,287
	Applicant(s): NAKATA, Shunji et al.	
	Filing Date: April 27, 2004	Group Art Unit: 2816

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA					
_____	AB					

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Translation (Yes or No)
<u>Ge</u>	AC 8-335873	12/17/1996	Japan	Abstract
<u>Ge</u>	AD 9-74347	03/18/1997	Japan	Abstract
<u>Ge</u>	AE 10-190442	07/21/1998	Japan	Abstract
<u>Ge</u>	AF 10-308662	11/17/1998	Japan	Abstract
_____	AG			

OTHER DOCUMENTS

<u>Ge</u>	AH	Patterson et al., "Structure and Design of a Computer, by David A. Patterson, and John L. Hennessy, published by NikkeiBP, September 22, 1997, page 677.
<u>Ge</u>	AI	Technical Report of Low Power LSI, Nikkei Micro-device, NikkeiBP, 1994, page 90.
<u>Ge</u>	AK	"A Low Power Multiplier Using Adiabatic Charging Binary Decision Diagram Circuit", <u>Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials</u> , Tokyo, 1999, pages 444-445.
<u>Ge</u>	AJ	Svensson et al., "Low Power Circuit Techniques", <u>Low Power Design Methodologies</u> , Kluwer Academic Publishers, 1996, Chapter 3, pages 37-52.
Examiner	Cassandra Cop	
Date Considered	January 7, 2005	



**INFORMATION
DISCLOSURE
CITATION
PTO-1449**

Atty. Docket No. 010704A

Serial No. 10/709,287

Applicant(s): NAKATA, Shunji et al.

Filing Date: April 27, 2004

Group Art Unit: 2816 (expected)

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	BA					
_____	BB					
_____	BC					
_____	BD					
_____	BE					

FOREIGN PATENT DOCUMENTS

Document No.	Date	Country	Translation (Yes or No)
_____	BF		
_____	BG		
_____	BH		

OTHER DOCUMENTS

<u>CX</u>	BI	Athas, William C., "Energy-Recovery CMOS", Low power Design Methodologies, J. M. Rabaey and M. Pedram (Kluwer Academic Publishers, 1996), Chapter 4, pages 65-72.
<u>Be</u>	BJ	Athas, William C. et al., "A Low-Power Microprocessor Based on Resonant Energy", IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997, pages 1693-1701.
<u>CXL</u>	BK	"Low Power and High Speed LSI Technology", Realize Co., along with partial translation of relevant parts, January 31, 1998.
Examiner	Date Considered	
<u>Cassandra Cox</u>	<u>January 7, 2005</u>	

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention

Adiabatic Charging Register Circuit

Application Number :

Confirmation Number:

First Named Applicant: Shunji NAKATA

Attorney Docket Number: 010704A

Art Unit:

Examiner:

Search string: (5473526 or 5521538 or 5900758 or 5994935 or 6046648 or 6313673 or 6323709).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
Se	1	5473526	1995-12-05	Svensson et al.		363	60
Se	2	5521538	1996-05-28	Dickinson		326	93
Se	3	5900758	1999-05-04	Kanno		327	201
Se	4	5994935	1999-11-30	Ueda et al.		327	202
Se	5	6046648	2000-04-04	Nakamiya et al.		331	116 FE
Se	6	6313673	2001-11-06	Watanabe	B1	327	115
Se	7	6323709	2001-11-27	Kulkarni et al.	B1	327	195

Signature

Examiner Name	Date
Cassandra Corp	January 7, 2005